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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,645	01/28/2004	Jin-ho Choi	SAM-0539	4437

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EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,645	CHOI ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-6* is/are rejected.

7)☒ Claim(s) *3,7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/28/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, and 4-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Roth et al. (U.S. 5,118,639).

With respect to claim 1, Roth et al. teaches a method of fabricating a local interconnection (column 7, lines 4-8) comprising forming a selective epitaxial growth seed layer pattern on a region of a semiconductor substrate where a local interconnection is to be formed (**32** in Fig. 4; column 4, lines 31-44); forming a selective epitaxial layer by performing epitaxial growth on the resultant structure (**38** and **40** in Fig. 5; column 5, lines 44-55; column 6, lines 16-19); and reducing a resistance of the selective epitaxial layer to complete the local interconnection (column 6, lines 36-44).

With respect to claim 2, Roth et al. teaches the method of claim 1, further comprising, prior to forming the selective epitaxial growth seed layer pattern, forming a shallow trench isolation structure on the semiconductor substrate to define an active region (**16** in Fig. 1; column 2, line 67 – column 3, line 5); forming a gate on the active region (**20** in Fig. 1; column 3, lines 14-18); and forming a spacer on a sidewall of the gate (column 4, lines 11-30), and wherein forming the selective epitaxial growth seed layer pattern comprises forming the selective epitaxial growth seed later pattern on the shallow trench isolation structure (Fig. 3; column 4, lines 31-37), and forming the

selective epitaxial layer comprises forming the selective epitaxial layer on the active region, the selective epitaxial growth seed pattern (column 5, lines 44-47), and the gate (column 4, lines 11-30: in the embodiment where sidewall spacers are fabricated on the gate electrode, encapsulation layer **26** is not present, and the epitaxial layer would form on the gate), and wherein the local interconnection comprises a local interconnection for connecting a source/drain region of a transistor to a source/drain region of an adjacent transistor (Fig. 6; column 8, lines 15-20).

With respect to claim 4, Roth et al. teaches the method of claim 1, wherein reducing the resistance of the selective epitaxial layer to complete the local interconnection comprises implanting ions into the selective epitaxial layer (column 6, lines 39-44).

With respect to claim 5, Roth et al. teaches the method of claim 1, wherein reducing the resistance of the selective epitaxial layer to complete the local interconnection comprises siliciding the selective epitaxial layer (column 6, lines 16-28).

With respect to claim 6, Roth et al. teaches the method of claim 1, wherein reducing the resistance of the selective epitaxial layer to complete the local interconnection comprises implanting ions into the selective epitaxial layer and siliciding the selective epitaxial layer (column 6, lines 19-26 teach siliciding the selective epitaxial layer, which, as taught in column 6, lines 36-44, can be doped in-situ during epitaxial growth or by ion implantation after the growth).

Allowable Subject Matter

Claims 3, 7, and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Prior art does not teach or suggest, in combination with the other claimed limitations, a method of fabricating a local interconnection comprising forming a selective epitaxial growth seed layer pattern, forming a selective epitaxial layer by performing epitaxial growth on the resultant structure, and reducing the resistance of the selective epitaxial layer, wherein the interconnect connects a source/drain region of a transistor to a gate of an adjacent transistor. Godinho et al. (U.S. 5,166,771) teaches a method of forming an interconnect between a source/drain region of a transistor and a gate of an adjacent transistor, but does not suggest forming an insulating layer pattern for exposing an active region adjacent the first gate and exposing the second gate, and forming a selective epitaxial growth seed layer on the insulating layer pattern, and forming a selective epitaxial layer on the active region adjacent the first gate, the selective epitaxial growth seed layer patter, and the second gate.

Prior art also does not teach or suggest, in combination with the other claimed limitations, a selective epitaxial growth seed layer comprised of $Si_xO_yN_z$. Chevalier et al. (U.S. 2002/0011001) teaches a method of using a patterned $Si_xO_yN_z$ layer to mask a selective epitaxial silicon growth, but does not suggest using it to seed the growth.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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